EPCET LIBRARY BANGALORE-49

CBCS SCHEME

USN | | | | | | | | | | |

21EC71

Seventh Semester B.E./B.Tech. Degree Examination, June/July 2026
Advanced VLSI

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Explain carry select adder and how it is extended to form n-bit Conditional SUM adder. **(10 Marks)**

b. With neat diagram, explain ASIC design **(10 Marks)**

OR

2 a. Explain Gate Array based logic. **(10 Marks)**

b. With relevant cell diagram and equations, explain 4 bit Carry Look Ahead Adder (CLA) **(10 Marks)**

Module-2

3 a. Explain I/O and Power planning in ASIC floor plan. **(10 Marks)**

b. Briefly explain the goals and objectives of the placement. **(05 Marks)**

c. Explain clock routing technique in brief. **(05 Marks)**

OR

4 a. Discuss the measurement of delay in floor plan. **(10 Marks)**

b. Write an algorithm for iterative placement improvement method and explain briefly. **(10 Marks)**

Module-3

5 a. What is Verification? List the steps in a test bench to determine the correctness of the design under test. **(10 Marks)**

b. Compare directed testing and constrained random test progress using a graph. **(10 Marks)**

OR

6 a. Explain :
(i) Associative arrays.
(ii) Dynamic Array with an example **(10 Marks)**

b. Using for each loop write program to print the following output :

0 :	0	1	2	3	4	5
1 :	10	11	12	13	14	15
2 :	20	21	22	23	24	25
3 :	30	31	32	33	34	35

(10 Marks)

Module-4

7 a. Write a sample code to declare a task and function, write the difference between task and function. **(10 Marks)**

b. Write and explain about separating the test bench and design. **(10 Marks)**

OR

8 a. What is Modport construct? Write an example program to show interface of test bench and monitor. **(10 Marks)**

b. What are all the main regions inside a system verilog time step? Explain. **(10 Marks)**

Module-5

9 a. Write a System Verilog Sample code to describe simple class (Packet class) with random visible constraints and test bench. **(10 Marks)**

b. Define the Randomization. Explain all the design inputs. **(10 Marks)**

OR

10 a. How do you measure coverage statistics during simulation? **(05 Marks)**

b. Write short note on coverage option. **(05 Marks)**

c. Write a system verilog code for basic cross coverage and also mention coverage summary report for basic cross coverage. **(10 Marks)**

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